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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number: 10/786,807
Filing Date: February 25, 2004
First Named Inventor: **HUI-MEI CHEN**
Art Unit: 2822
Examiner Name: **BAC H. AU**

Sheet 1 of 3

Attorney Docket No: 085027-0106

US PATENT DOCUMENTS

Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or RelevantFigures Appear
		NONE			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or RelevantFigures Appear	T[2]
		NONE				

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
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	4	GAO, X. et al. "An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance," Solid-State Electronics, 27 (2003), pgs. 1105-1110	
	5	YEOH, A. et al. "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing," Electronic Components and Technology Conference (2006) pgs. 1611-1615	
	6	HU, C-K. et al. "Copper-Polyimide Wiring Technology for VLSI Circuits," Materials Research Society Symposium Proceedings VLSI V (1990) pgs. 369-373	
	7	ROESCH, W. et al. "Cycling copper flip chip interconnects," Microelectronics Reliability, 44 (2004) pgs. 1047-1054	

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	8	LEE, Y-H. et al. "Effect of ESD Layout on the Assembly Yield and Reliability," International Electron Devices Meeting (2006) pgs. 1-4	
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	21	GEFFKEN, R. M. "An Overview of Polyimide Use in Integrated Circuits and Packaging," Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology (1991) pgs. 667-677	
	22	LUTHER, B. et al. "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices," Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference (1993) pgs. 15-21	
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	25	LIN, M.S. et al. "A New System-on-a-Chip (SOC) Technology – High Q Post Passivation Inductors," Proceedings from the 53rd Electronic Components and Technology Conference (05-30-2003) pgs. 1503-1509	
	26	MEGIC CORP. "MEGIC way to system solutions through bumping and redistribution," (Brochure) (02-06-2004) pgs. 1-3	
	27	LIN, M.S. "Post Passivation Technology™ - MEGIC ® Way to System Solutions," Presentation given at TSMC Technology Symposium, Japan (10-01-2003) pgs. 1-32	
	28	LIN, M.S. et al. "A New IC Interconnection Scheme and Design Architecture for High Performance ICs at Very Low Fabrication Cost – Post Passivation Interconnection," Proceedings of the IEEE Custom Integrated Circuits Conference (09-24-2003) pgs. 533-536	

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